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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/829,646 | 04/21/2004 | Mark Klecka | 54606 | 7083 |

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The Law Offices of Calvin B. Ward
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| EXAMINER | |
|---|---|
| TSAI, HENRY | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2181 | |

DATE MAILED: 05/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/829,646 | KLECKA ET AL. | |
| | Examiner | Art Unit | |
| | Henry W.H. Tsai | 2181 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *4/21/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *4/21/04* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

**DETAILED ACTION**

. ***Claim Rejections - 35 USC § 102***

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-9 are rejected under 35 U.S.C. 102(e) as being anticipated by Zeitler et al. (U.S. Patent Application Publication No.2004/0210693), herein referred to as Zeitler et al.'693.

Referring to claim 1, Zeitler et al.'693 discloses, as claimed, a circuit (see Fig. 1A or 1B) comprising: a plurality of processing blocks (interconnection controller 230, see Fig.

2) on a first substrate (such as cluster 101, see Fig. 1A); and an interconnect network comprising a plurality of network nodes (processors 202a-202d, see Fig. 2) arranged in a two-dimensional array on said first substrate, each network node having a plurality of adjacent network nodes (processors 202a-202d, see Fig. 2) and being connected to each adjacent network node by a communication bus (208a-208e, see Fig. 2) that connects only those two network nodes and processing blocks adjacent to that bus (note processors 202a has adjacent processors 202b and 202c, see Fig. 2); each network node (202 see Fig. 4) comprising: a plurality of communication ports (404a-404c, see Fig. 4), each communication port comprising an input port (input ports in each of 404a-404c, see Fig. 4) for receiving digital signals and an output port (output ports in each of 404a-404c, see Fig. 4) for transmitting digital signals (such as CLK, CTL, and CASD (n:0), see Fig. 4) on a bus connected to that communication port; a programmable switch (the switch inside Zeitler et al.'693's processor 202 using routing tables 406a-406c, see Fig. 4) that selectively connects one of said input ports to one of said output ports in response to connection information (see paragraph [0036], lines 1-3, regarding information in the associated routing tables) stored in a memory (routing tables 406a-406c, see paragraph [0036], lines 1-3) in that network

node, wherein; each processing block (interconnection controller 230, see Fig. 2) is connected to one of said communication buses (208a-208e, see Fig. 2) and sends and/or receives data on that bus, each processing block performing a predetermined processing function (see paragraph [0027], lines 4-8, regarding interconnection controller 230 performs a variety of functions), said processing block being located within said two-dimensional array of network nodes (processors 202a-202d, see Fig. 2).

As to claim 2, Zeitler et al.'693 also discloses: the circuit of claim 1 wherein said connection information is stored in said network nodes (see paragraph [0036], lines 1-3, regarding information in the associated routing tables) prior to said processing blocks commencing said processing functions.

As to claim 3, Zeitler et al.'693 also discloses: the circuit of claim 1 further comprising a programming bus (208a-208e, see Fig. 2) for transmitting said connection information to each of said network nodes (processors 202a-202d, see Fig. 2).

As to claim 4, Zeitler et al.'693 also discloses: the circuit of claim 1 wherein each of said buses (208a-208e, see Fig. 2) is a serial bus.

As to claim 5, Zeitler et al.'693 also discloses: the circuit of claim 1 wherein said two dimensional array (see Figs.

1A, 1B, and 2) comprises a rectangular array in which said network nodes are organized as a plurality of rows and columns.

As to claim 6, Zeitler et al.'693 also discloses: the circuit of claim 1 further comprising: a second substrate (such as cluster 105, see Fig. 1A) that overlies said first substrate, said second substrate comprising an interconnect network comprising a plurality of network nodes (processors 202a-202d, see Fig. 2) arranged in a two-dimensional array on said second substrate, each network node having a plurality of adjacent network nodes (processors 202a-202d, see Fig. 2) and being connected to each adjacent network node by a communication bus (208a-208e, see Fig. 2) that connects only those two network nodes (note processors 202a has adjacent processors 202b and 202c, see Fig. 2); each network node comprising: a plurality of communication ports (404a-404c, see Fig. 4), each communication port comprising an input port (input ports in each of 404a-404c, see Fig. 4) for receiving digital signals and an output port (output ports in each of 404a-404c, see Fig. 4) for transmitting digital signals (such as CLK, CTL, and CASD (n:0), see Fig. 4) on a bus connected to that communication port; a programmable switch (the switch inside Zeitler et al.'693's processor 202 using routing tables 406a-406c, see Fig. 4) that selectively connects one of said input ports to one of said output ports in

response to connection information stored in a memory (routing tables 406a-406c, see paragraph [0036], lines 1-3) in that network node, wherein at least one of said network nodes (processors 202a-202d, see Fig. 2) on said second substrate is connected to a corresponding network node (processors 202a-202d, see Fig. 2) on said first substrate by a bus (111a, see Fig. 1A) that connects only those two network nodes (processors 202a-202d, see Fig. 2).

As to claim 7, Zeitler et al.'693 also discloses: the circuit of claim 1 wherein one of said processing blocks (interconnection controller 230, see Fig. 2) specifies said connection information (see paragraph [0036], lines 1-3, regarding information in the associated routing tables) that is stored in each of said network nodes.

As to claim 8, Zeitler et al.'693 also discloses: the circuit of claim 7 wherein said one of said processing blocks (interconnection controller 230, see Fig. 2) also comprises an interface (I/O 216 or I/O 220, see Fig. 2) for receiving said connection information from a source external to said circuit.

As to claim 9, Zeitler et al.'693 also discloses: the circuit of claim 1 wherein one of said processing blocks (interconnection controller 230, see Fig. 2) is a spare processing block that is capable of performing processing

functions that are normally performed by a second one of said processing blocks (interconnection controller 230, see Fig. 2) if said second one of said processing blocks is defective (see paragraph [0027], lines 4-14, regarding interconnection controller 230 performs a variety of functions; and there can be more than one interconnection controller 230 in one cluster).

***Conclusion***

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Mancusi et al. discloses each port module includes a plurality of ports which can be programmed to electrically couple selected sets of the plurality of network components without physically rerouting network cabling.

Ouellet al. discloses an interconnect uses a lightweight protocol with control characters embedded into the data stream. The control characters define events such as end of packet, end of packet with error, transmit on, transmit off, synchronizing codes, and pass-through status.

Trussellet al. discloses: each node can be configured from a variety of modular subsystems on a common bus including

modules for network control, data acquisition, digital and analog inputs and outputs, display terminals and the like in accordance with system requirements.

***Contact Information***

**4.** Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (571) 272-4176. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Fritz M. Fleming, can be reached on (571) 272-4145. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to **the TC central telephone number, 571-272-2100.**

5. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into **the Group at fax number: 571-273-8300.** This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account.

Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER
May 3, 2006